CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. An apparatus for operating a content addressable memory (CAM) device comprising:

an encoding circuit for encoding an incoming CAM word to produce an encoded CAM word such that a one-bit mismatch between a comparand and said incoming CAM word results in at least a M-bit mismatch between said encoded CAM word and a similarly encoded comparand;

a circuit for precharging a match line to a predetermined state before a comparison between said encoded CAM word and said similarly encoded comparand; and

a memory storage location for storing said encoded CAM word.

2. The apparatus according to claim 1, wherein said encoding circuit further comprises:

a masking device for masking a prefix of said loaded CAM word;

a shift register for shifting said masked CAM word; and

an exclusive-OR wire-OR (XOR-WOR) gate for performing an XOR-WOR operation between said masked CAM word and said shifted CAM word.

3. The apparatus according to claim 2, wherein said masking device further comprises a test/load bus for storing a result of said XOR-WOR operation in said memory storage location.

4. The apparatus according to claim 2, wherein said masking device further comprises:

a bit enable store assigned to a bit of said prefix of said loaded CAM word for controlling said masking of said CAM word; and

an AND gate for masking said bit of said prefix of said CAM word in accordance with said bit enable store.

5. The apparatus according to claim 2, wherein said shift register shifts said masked CAM word right one bit.

6. The apparatus according to claim 2, wherein said masking device further comprises:

a program position value register for decoding and selecting which bits of said prefix of said loaded CAM word are masked; and

an AND gate for masking said bits of said prefix of said CAM word in accordance with said program position value register.

7. The apparatus according to claim 2, wherein said shifted CAM word is padded with zeros.

8. The apparatus according to claim 2, wherein said encoding circuit further comprises:

a masking device for masking a prefix of said comparand;

a shift register for shifting said masked comparand; and

an exclusive-OR wire-OR (XOR-WOR) gate for performing an XOR-WOR operation between said masked comparand and said shifted comparand, said encoded comparand being compared to said encoded CAM word.

9. The apparatus according to claim 8, wherein said masking device further comprises:

a bit enable store assigned to a bit of said prefix of said comparand for controlling said masking of said comparand; and

an AND gate for masking said bit of said prefix of said comparand in accordance with said bit enable store.

10. The apparatus according to claim 8, wherein said shift register shifts said masked CAM word right one bit.

11. The apparatus according to claim 8, wherein said masking device further comprises:

a program position value register for decoding and selecting which bits of said prefix of said comparand are masked; and

an AND gate for masking said bits of said prefix of said comparand in accordance with said program position value register.

12. The apparatus according to claim 1, wherein said encoding circuit implements an error correcting code.

13. The apparatus according to claim 12, wherein said error correcting code has a Hamming distance greater than one.

14. An apparatus for operating a ternary content addressable memory (TCAM) device comprising:

a masking device for producing a masked TCAM word by masking off all bits in an incoming TCAM word that are not used in a matching prefix;

an encoding circuit for encoding said masked TCAM word to produce an encoded TCAM word such that a one-bit mismatch between a comparand and said incoming TCAM word results in at least a M-bit mismatch between said encoded TCAM word and a similarly encoded comparand;

a circuit for precharging a match line to a predetermined state before a comparison between said encoded TCAM word and said similarly encoded comparand; and

a memory storage location for storing said encoded TCAM word.

15. The apparatus according to claim 14, wherein said TCAM device comprises a plurality of hierarchical of blocks.

16. The apparatus according to claim 15, wherein each word of each block of said TCAM device has a same prefix length.

17. The apparatus according to claim 14, wherein said shifted TCAM word is padded with don't care values.

18. The apparatus according to claim 14, wherein said encoding circuit further comprises:

a shift register for shifting said masked TCAM word; and

an exclusive-OR wire-OR (XOR-WOR) gate for performing an XOR-WOR operation between said masked TCAM word and said shifted TCAM word.

19. The apparatus according to claim 18, wherein said masking device further comprises a test/load bus for storing a result of said XOR-WOR operation in said memory storage location.

20. The apparatus according to claim 18, wherein said masking device further comprises:

a bit enable store assigned to a bit of said prefix of said loaded TCAM word for controlling said masking of said TCAM word; and

an AND gate for masking said bit of said prefix of said TCAM word in accordance with said bit enable store.

21. The apparatus according to claim 18, wherein said shift register shifts said masked TCAM word right one bit.

22. The apparatus according to claim 18, wherein said masking device further comprises:

a program position value register for decoding and selecting which bits of said prefix of said loaded TCAM word are masked; and

an AND gate for masking said bits of said prefix of said TCAM word in accordance with said program position value register.

23. The apparatus according to claim 18, wherein said encoding circuit further comprises:

a masking device for masking a prefix of said comparand;

a shift register for shifting said masked comparand; and

an exclusive-OR wire-OR (XOR-WOR) gate for performing an XOR-WOR operation between said masked comparand and said shifted comparand, said encoded comparand being compared to said encoded TCAM word.

24. The apparatus according to claim 23, wherein said masking device further comprises:

a bit enable store assigned to a bit of said prefix of said comparand for controlling said masking of said comparand; and

an AND gate for masking said bit of said prefix of said comparand in accordance with said bit enable store.

25. The apparatus according to claim 23, wherein said shift register shifts said masked TCAM word right one bit.

26. The apparatus according to claim 23, wherein said masking device further comprises:

a program position value register for decoding and selecting which bits of said prefix of said comparand are masked; and

an AND gate for masking said bits of said prefix of said comparand in accordance with said program position value register.

27. The apparatus according to claim 14, wherein said encoding circuit implements an error correcting code.

28. The apparatus according to claim 27, wherein said error correcting code has a Hamming distance of two.

29. A processing system comprising:

a processor;

a content addressable memory (CAM) device coupled to said processor via a bus, said CAM device comprising an apparatus for operating said CAM device, said apparatus comprising:

an encoding circuit for encoding an incoming CAM word to produce an encoded CAM word and having the property that a one-bit mismatch between a comparand and said incoming CAM word will produce at least a two-bit mismatch between said encoded CAM word and a similarly encoded comparand;

a circuit for precharging a match line to a predetermined state before a comparison between said encoded CAM word and said similarly encode comparand; and

a memory storage location for storing said encoded CAM word.

30. A processing system comprising:

a processor;

a ternary content addressable memory (TCAM) device coupled to said processor via a bus, said TCAM device comprising an apparatus for operating said TCAM device, said apparatus comprising:

a masking circuit for producing a masked TCAM word by masking off all bits in an incoming TCAM word that are not used in a matching prefix;

an encoding circuit for encoding said masked TCAM word to produce an encoded TCAM word such that a one-bit mismatch between a comparand and said incoming TCAM word results in at least a two-bit mismatch between said encoded TCAM word and a similarly encoded comparand;

a circuit for precharging a match line to a predetermined state before a comparison between said encoded TCAM word and said similarly encode comparand; and

a memory storage location for storing said encoded TCAM word.

31. A method for operating a content addressable memory (CAM) device comprising:

encoding an incoming CAM word to produce an encoded CAM word such that a one-bit mismatch between a comparand and said incoming CAM word results in at least an M-bit mismatch between said encoded CAM word and a similarly encoded comparand;

precharging a match line to a predetermined state before a comparison between said encoded CAM word and said encoded comparand; and

storing said encoded CAM in a memory storage location of said CAM device.

32. The method according to claim 31, further comprising:

masking a prefix of said loaded CAM word;

shifting said masked CAM word; and

performing an exclusive-OR wire-OR (XOR-WOR) operation between said masked CAM word and said shifted CAM word.

33. The method according to claim 32, further comprising:

controlling said masking of said prefix of said CAM word using a bit assigned for that purpose; and

performing an AND operation to mask said prefix of said CAM word in accordance with said controlling bit.

34. The method according to claim 32, wherein said shifting said masked CAM word right one bit.

35. The method according to claim 32, wherein said masking further comprises:

decoding and selecting which bits of said prefix of said loaded CAM word are masked; and

performing an AND operation in order to mask said bits of said prefix of said CAM word in accordance with said decoding and selecting.

36. The method according to claim 32, wherein said shifted CAM word is padded with zeros.

37. The method according to claim 32, further comprising:

masking a prefix of said comparand;

shifting said masked comparand;

performing an XOR-WOR operation between said masked comparand and said shifted comparand; and

comparing said encoded comparand to said encoded CAM word.

38. The method according to claim 37, wherein said masking device further comprises:

controlling said masking of said prefix of said comparand using a bit assigned for that purpose; and

performing an AND operation to mask said prefix of said comparand in accordance with said controlling bit.

39. The method according to claim 37, wherein said shifting said masked CAM word right one bit.

40. The method according to claim 37, wherein said masking further comprises:

decoding and selecting which bits of said prefix of said comparand are masked; and

performing an AND operation in order to mask said bits of said prefix of said comparand in accordance with said decoding and selecting.

41. The method according to claim 32, wherein said encoding is performed using an error correcting code.

42. The method according to claim 41, wherein said error correcting code has a Hamming distance greater than one.

43. A method for operating a ternary content addressable memory (TCAM) device comprising:

masking off all bits in an incoming TCAM word that are not used in a matching prefix to produce a masked TCAM word;

encoding said masked TCAM word to produce an encoded TCAM word such that a one-bit mismatch between a comparand and said incoming TCAM word results in at least a two-bit mismatch between said encoded TCAM word and a similarly encoded comparand;

precharging a match line to a predetermined state before a comparison between said encoded TCAM word and said encoded comparand; and

storing said encoded TCAM in a memory storage location of said TCAM device.

44. The method according to claim 43, wherein said TCAM device comprises a plurality of hierarchal blocks.

45. The method according to claim 44, wherein each word of each block of said TCAM device has a same prefix length.

46. The method according to claim 43, wherein said shifted TCAM word is padded with don't care values.

47. The method according to claim 43, further comprising:

shifting said masked TCAM word; and

performing an exclusive-OR wire-OR (XOR-WOR) operation between said masked TCAM word and said shifted TCAM word.

48. The method according to claim 47, further comprising:

controlling said masking of said prefix of said TCAM word using a bit assigned for that purpose; and

performing an AND operation to mask said prefix of said TCAM word in accordance with said controlling bit.

49. The method according to claim 47, wherein said shifting said masked TCAM word right one bit.

50. The method according to claim 47, wherein said masking further comprises:

decoding and selecting which bits of said prefix of said loaded TCAM word are masked; and

performing an AND operation in order to mask said bits of said prefix of said TCAM word in accordance with said decoding and selecting.

51. The method according to claim 43, further comprising:

masking a prefix of said comparand;

shifting said masked comparand;

performing an XOR-WOR operation between said masked comparand and said shifted comparand; and

comparing said encoded comparand to said encoded TCAM word.

52. The method according to claim 51, wherein said masking further comprises:

controlling said masking of said prefix of said comparand using a bit assigned for that purpose; and

performing an AND operation to mask said prefix of said comparand in accordance with said controlling bit.

53. The method according to claim 47, wherein said shifting said masked TCAM word right one bit.

54. The method according to claim 47, wherein said masking further comprises:

decoding and selecting which bits of said prefix of said comparand are masked; and

performing an AND operation in order to mask said bits of said prefix of said comparand in accordance with said decoding and selecting.

55. The method according to claim 43, wherein said encoding is performed using an error correcting code.

56. The method according to claim 55, wherein said error correcting code has a Hamming distance of two.